CLAIM AMENDMENTS

IN THE CLAIMS

This listing of the claims will replace all prior versions, and listing, of claims in the application or previous response to office action:

1. (Currently Amended) A distributed memory test system comprising:

a host computer ~~having one or more~~ storing a plurality of different test recipes;

plural test sites distributed distal from the host computer, each test site adapted to interface with a memory device under test, each test site having an embedded processor; and

a network interfaced with the host computer and the plural test sites, the network communicating ~~the~~ respective test recipes ~~test recipe~~ from the host computer to respective embedded processors ~~the embedded processor~~ for execution ~~of the test recipe by the test site~~ by respective test sites, wherein the host computer provides at least one of the test sites with a test recipe different from a recipe provided to another test site.

2. (Original) The system of Claim 1 wherein the memory device under test comprises a flash memory device.

3. (Original) The system of Claim 1 wherein the memory device under test comprises a fast page DRAM.

4. (Original) The system of Claim 1 wherein the memory device under test comprises an EDO DRAM.

5. (Original) The system of Claim 1 wherein the memory device under test comprises a SDRAM.

6. (Original) The system of Claim 1 wherein the memory device under test comprises a DDR.

7. (Cancelled)

8. (Original) The system of Claim 1 wherein the memory device under test comprises a SRAM.

9. (Original) The system of Claim 1 wherein the memory device under test comprises a EEPROM.

10. (Original) The system of Claim 1 wherein the network comprises Ethernet.

11. (Original) The system of Claim 10 wherein the test recipe comprises XML formatted data.

12. (Original) The system of Claim 11 wherein each embedded processor accepts the XML formatted recipe data to generate instructions for testing the memory device under test.

13. (Original) The system of Claim 1 wherein the network comprises a local area network.

14. (Original) The system of Claim 1 wherein the network comprises the internet.

15. (Original) The system of Claim 14 wherein the test recipe comprises XML formatted data communicated from the host computer to a test site using TCP/IP.

16. (Original) The system of Claim 14 wherein the test recipe comprises XML formatted data communicated from the host computer to a test site using NFS.

17. (Original) The system of Claim 1 wherein the test recipe comprises instructions for performing algorithmic testing at the test site.

18. (Original) The system of Claim 1 wherein the test recipe comprises instructions for performing vector testing at the test site.

19. (Original) The system of Claim 1 further comprising:

plural host computers interfaced with the network, each host computer having one or more test recipes;

wherein each host computer controls tests performed by at least one test site.

20. (Original) The system of Claim 19 further comprising a test designer interfaced with the network, the test designer operational to create the test recipes and communicate the test recipes to the host computers.

21. (Currently Amended) A method for testing memory devices, the method comprising:

communicating a first test recipe from a host computer over a network to a first test site;

communicating a second test recipe, different from the first test recipe, from a host computer over a network to a second test site;

translating the test recipes ~~recipe with a processor~~ at the respective test ~~site~~ sites into test instructions; and

testing respective ~~a~~ memory devices ~~device~~ at the respective test sites ~~site~~ in accordance with the instructions.

22. (Original) The method of Claim 21 wherein communicating further comprises sending the test recipe as XML formatted data.

23. (Original) The method of Claim 22 wherein the network comprises Ethernet.

24. (Original) The method of Claim 22 wherein the network comprises a local area network.

25. (Original) The method of Claim 22 wherein the network comprises the internet.

26. (Original) The method of Claim 22 wherein the network comprises a wide area network.

27. (Original) The method of Claim 22 wherein sending the XML formatted data further comprises sending the data using TCP/IP.

28. (Original) The method of Claim 22 wherein sending the XML formatted data further comprises sending the data using NFS.

29. (Original) The method of Claim 27 wherein the XML formatted data is downloaded from the host to the test site by FTP.

30. (Original) The method of Claim 21 wherein translating the test recipe further comprises:

reading the test recipe with a processor at the test site;

associating the recipe with instructions stored at the test site;

executing the associated instructions to generate test data for storage on the memory device;

reading the data from the memory device; and

comparing the read data with a predetermined result to determine whether the memory device accurately stores data.

31. (Original) The method of Claim 30 further comprising:

formatting the results from the comparing step into XML formatted data; and

sending the results to the host computer.

32. (Original) The method of Claim 30 wherein the executing step comprises executing the instructions with a sequencer at the test site.

33. (Cancelled)

34. (Currently Amended) The method of Claim [[33]] 30 wherein the instructions call vectors from vector memory stored at the test site.

35. (Original) The method of Claim 34 wherein the test data comprises address data and storage data, the address data generated algorithmically and the storage data called from vector memory.

36. (Original) The method of Claim 34 wherein the test data comprises address data and storage data, the storage data generated algorithmically and the address data called from vector memory.

37. (Currently Amended) An apparatus for testing a memory device, the apparatus comprising:

an adapter for physical interfacing with the memory device under test;

a test engine interfaced with the adapter to send test data to the memory device according to test instructions and to read stored data from the memory device for comparison with predetermined results, wherein the test instructions comprise instructions to perform vector testing; and

a processor interfaced with the test engine and adapted to interface with a network, the processor operable to receive a test recipe from the network and to translate the test recipe into test instructions for execution by the test engine.

38. (New) The apparatus of Claim 37, wherein the test engine comprises a sequencer.

39. (New) The apparatus of Claim 37, wherein the test instructions comprise:
instructions to call storage data from vector memory; and
instructions to algorithmically generate address data.

40. (New) The apparatus of Claim 37, wherein the test instructions comprise:
instructions to call address data from vector memory; and
instructions to algorithmically generate storage data.

41. (New) A distributed memory test system comprising:
a host computer having one or more test recipes;
plural test sites distributed distal from the host computer, each test site adapted to interface with a memory device under test, each test site having an embedded processor; and
a network interfaced with the host computer and the plural test sites, the network communicating the test recipe from the host computer to the embedded processor for execution of the test recipe by the test site, wherein the test recipe comprises instructions for performing vector testing at the test site.

42. (New) A method for testing memory devices, the method comprising:

communicating a test recipe from a host computer over a network to a test site;

translating the test recipe with a processor at the test site into test instructions; and

testing a memory device at the test site in accordance with the instructions, wherein the instructions call vectors from vector memory stored at the test site.

43. (New) The method of Claim 42, further comprising:

calling storage data from vector memory; and

generating address data algorithmically.

44. (New) The method of Claim 42, further comprising:

calling address data from vector memory; and

generating storage data algorithmically.

45. (New) The method of Claim 1, wherein each of the test recipes comprises test parameters.

46. (New) The method of Claim 45, wherein different test recipes comprise common production recipes and different test parameters.

47. (New) The method of Claim 21, wherein the first test recipe is different than the second test recipe at least because the first and second test recipe comprise different test parameters.